Electronic Version

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Description

[THREE-DIMENSIONAL MEMORY STRUCTURE AND MANUFACTURING METHOD THEREOF]

BACKGROUND OF INVENTION

[0001] Field of Invention

[0002] The present invention relates to a three-dimensional memory structure and manufacturing method thereof. More particularly, the present invention relates to a vertically stacked three-dimensional memory array and manufacturing method thereof.

[0003] Description of Related Art

[0004]

Due to the rapid development of integrated circuit technologies, each integrated circuit contains an increasing number of electronic devices. Memory is a common semiconductor device most often used inside a personal computer and some electronic equipment. Earlier, each memory includes an array of memory cells on a single layer over a semiconductor substrate. The cross over area between each column and row constitutes a specified memory cell address. In general, memory cells within the same column or the same row have a common

conductive wire connection. With this design, the only way to increase the level of integration is to reduce the size of each memory cell. A vertical stacked non-volatile memory structure is disclosed in U.S. Patent No. 6,351,406. The method includes forming a three-dimensional multi-layered array memory structure over a substrate with each array layer having a plurality of memory cells such that the memory cells in the same column or row are connected to a common conductive wire.

[0005] Fig. 1 is a front view of a conventional three-dimensional multi-layered memory array structure. As shown in Fig. 1, if a first patterned conductive layer 1 lies in an east/west direction and a second patterned conductive layer 3 lies in a south/north direction above the first patterned conductive layer 1, a cylindrical memory cell 5 is formed in the area of intersection between the vertical projection of the second patterned conductive layer 3 and the first patterned conductive layer 1. Furthermore, if a third patterned conductive layer 7 lies in an east/west direction, a cylindrical memory cell 9 is formed in the area of intersection between the vertical projection of the third patterned conductive layer 7 and the second patterned conductive layer 3. In other words, according to the aforementioned stacking method, even-numbered patterned conductive layers lie in a south/north direction and odd-numbered patterned conductive layers lie in an east/west direction.

[0006] Although U.S. Patent No. 6,351,406 has proposed a method of manufacturing a vertical stacked non-volatile memory for increasing

overall level of device integration, the method requires N+1 photolithographic processes to form the N memory cell array layers over a substrate. Along with the photolithographic steps needed to producing interconnecting vias, the total number of processing steps is exceptionally high. In other words, the stacked three-dimensional memory is rather difficult and costly to manufacture.

SUMMARY OF INVENTION

[0007] Accordingly, one object of the present invention is to provide a three-dimensional memory structure and manufacturing method thereof that only involves simple processing steps.

[0008] A second object of this invention is to provide a three-dimensional memory structure and manufacturing method thereof capable of increasing overall level of integration of the memory devices.

[0009] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a three-dimensional memory structure. The memory structure comprises a multiple of stacked circuits. The first stacked circuit includes two conductive layers, an n-type polysilicon layer, a p-type polysilicon layer and an anti-fuse. The n-type polysilicon layer in the first stacked circuit is located between the two conductive layers and the p-type polysilicon layer is located between the n-type polysilicon layer and one of the two conductive layers. The anti-fuse is located between the n-type polysilicon layer and the other one of the two conductive layers. Hence, the first stacked circuit includes a

conductive layer/p-type polysilicon layer/n-type polysilicon layer/anti-fuse/conductive layer (C/P/N/A/C) setup and a conductive layer/anti-fuse/n-type polysilicon layer/p-type polysilicon layer/conductive layer (C/A/N/P/C) setup.

[0010] The second stacked circuit of the three-dimensional memory structure includes two conductive layers, an n-type polysilicon layer, a p-type polysilicon layer and an anti-fuse. The p-type polysilicon layer of the second stacked circuit is located between the two conductive layers and the n-type polysilicon layer is located between the p-type polysilicon layer and one of the conductive layers. The anti-fuse is located between the p-type polysilicon and the other one of the two conductive layers. Hence, the second stacked circuit includes a conductive layer/anti-fuse/p-type polysilicon layer/n-type polysilicon layer/conductive layer (C/A/P/N/C) setup and a conductive layer/n-type polysilicon layer/p-type polysilicon layer/anti-fuse/conductive layer (C/N/P/A/C) setup. The second stacked circuit and the first stacked circuit cross over each other in the vertical dimension. Therefore, a total of four different methods of combining the first stacked circuit and the second stacked circuit are possible. In addition, according to the memory capacity, one of the four aforementioned configurations can be used to form more stacked circuits over the substrate.

[0011] This invention also provides a method of fabricating a three-dimensional memory structure. First, an n-type polysilicon layer/conductive layer/anti-fuse/n-type polysilicon layer (N/C/A/N) stack

structure is formed over a substrate. The N/C/A/N stack structure is patterned to form an array of linear first stacked lines. Thereafter, a dielectric layer is formed in the space between the first stacked lines above the substrate. The dielectric layer is planarized to expose the topmost n-type polysilicon layer of the first stacked lines. A p-type polysilicon/conductive layer/anti-fuse/p-type polysilicon layer (P/C/A/P) stacked structure is formed over the topmost n-type polysilicon layer of the first stacked line. Next, the P/C/A/P stacked structure and the topmost n-type polysilicon layer of the first stacked line is patterned to form an array of linear second stacked lines that crosses over the first stacked lines vertically. Another dielectric layer is formed in the space between the second stacked lines above the anti-fuse of the first stacked lines. The dielectric layer is again planarized to expose the topmost p-type polysilicon layer of the second stacked lines. The overlapping areas between the first stacked lines and the second stacked lines forms an array of cylindrical memory cells. The aforementioned processing steps are repeated to form more stacked lines and hence build up a three-dimensional memory structure.

[0012]

A three-dimensional multi-layered memory array structure is used in this invention. The odd-numbered memory cell array and the even-numbered memory cell array of the three-dimensional structure are alternately stacked over each other and oriented in a direction perpendicular to each other above the substrate. Hence, substrate area required to accommodate the memory device is reduced and overall

level of integration of the memory chip is increased. Moreover, in the fabrication process, the anti-fuse is used as an etching stop layer. Since the anti-fuse is fabricated from silicon oxide, the anti-fuse has a relatively high etching selectivity ratio relative to the polysilicon and the conductive layer. Therefore, the processing window is increased and the steps for fabricating the three-dimensional memory are simplified. Furthermore, the steps of forming via is to break through the anti-fuse after etching stop on the anti-fuse, so it can effectively etch stop on the conductive layer. Therefore, it can prevent via from forming p-n or n-p rectification junction due to the conductive layer being perforated, resulting in non-conducting.

[0013] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0014] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0015] Fig. 1 is a front view of a conventional three-dimensional multi-layered memory array structure.

[0016]

Figs. 2A and 2B are front views and side view of a three-dimensional

memory structure according to one preferred embodiment of this invention.

[0017] Figs. 3A to 3G are front views showing the progression of steps for forming the three-dimensional memory structure shown in Figs. 2A and 2B.

[0018] Figs. 4A to 4G are side views that correspond with the front views shown in Figs. 3A to 3G.

DETAILED DESCRIPTION

[0019] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0020]

Figs. 2A and 2B are front views and side view of a three-dimensional memory structure according to one preferred embodiment of this invention. As shown in Figs. 2A and 2B, the three-dimensional structure comprises of a stack of circuit layers. The first stack circuit 21 includes two n-type polysilicon layers 23 and 25, a conductive layer 27 and an anti-fuse 29. The anti-fuse 29 is a silicon oxide layer and the conductive layer 27 is a tungsten silicide or a titanium silicide layer, for example. The conductive layer 27 of the first stack circuit 21 is located between the two n-type polysilicon layers 23 and 25. The anti-fuse 29 is located between the n-type polysilicon layer 25 and the conductive layer 27.

Hence, the first stack circuit 21 has an n-type polysilicon/conductive layer/anti-fuse/n-type polysilicon (N/C/A/N) setup. The second stack circuit 31 of the three-dimensional memory structure includes two p-type polysilicon layers 33 and 35, another conductive layer 37, another anti-fuse 39 and the n-type polysilicon layer 25 of the first stack circuit. The conductive layer 37 of the second stack circuit 31 is located between the p-type polysilicon layer 33 and 35. The anti-fuse 39 is located between the p-type polysilicon layer 35 and the conductive layer 37. Hence, the second stack circuit 31 has a p-type polysilicon/conductive layer/anti-fuse/p-type polysilicon (P/C/A/P) setup. The second stack circuit 31 crosses over the first stack circuit 21 vertically. In this invention, memory capacity of the three-dimensional structure depends on the number of stack circuits over the substrate. Hence, stacking more circuits on top of the substrate will increase the overall memory capacity.

[0021] In general, there are other types of setups for the various layers inside the aforementioned stack circuit. For example, the first stack circuit 21 can have an n-type polysilicon/anti-fuse/conductive layer/n-type polysilicon (N/A/C/N) setup and the second stack circuit 31 can have a p-type polysilicon/anti-fuse/conductive layer/p-type polysilicon setup. In fact, there are four different setups for combining the first stack circuit 21 and the second stack circuit 31 together.

[0022] Figs. 3A to 3G are front views showing the progression of steps for forming the three-dimensional memory structure shown in Figs. 2A and

2B. Figs. 4A to 4G are side views that correspond with the front views shown in Figs. 3A to 3G. As shown in Figs. 3A and 4A, a substrate 200 such as a silicon substrate is provided. Thereafter, an n-type polysilicon layer 202, a conductive layer 204, an anti-fuse 206 and another n-type polysilicon layer 208 are sequentially formed over the substrate 200. The n-type polysilicon layer 202 and 208 are formed, for example, by conducting an in-situ doping using phosphene as a gaseous source. The conductive layer 204 is a tungsten silicide layer or a titanium silicide layer, for example. The conductive layer 204 is formed, for example, by conducting a low-pressure chemical vapor deposition. The anti-fuse 206 is fabricated using a material having an etching selectivity ratio higher than the n-type polysilicon layers 202, 208 and the conductive layer 204 including, for example, silicon oxide. The anti-fuse 206 is formed, for example, by conducting a low-pressure chemical vapor deposition.

[0023]

The n-type polysilicon layer 202, the conductive layer 204, the anti-fuse 206 and the n-type polysilicon layer 208 are patterned to form an array of linear first stack circuits 210 each having an n-type polysilicon/conductive layer/anti-fuse/n-type polysilicon (N/C/A/N) composite layer setup. Thereafter, a dielectric layer 10 is formed in the space between the first stack circuits 210. The dielectric layer 10 is, for example, a silicon oxide layer, a silicon nitride layer or a spin-coated glass layer. The dielectric layer 10 is formed, for example, by performing a high-density plasma chemical vapor deposition or a spin-

coating process.

[0024] A portion of the dielectric layer 10 is removed to expose the topmost n-type polysilicon layer 208. The dielectric layer 10 above the n-type polysilicon layer 208 is removed, for example, by chemical-mechanical polishing or conducting an etching back process.

[0025] As shown in Figs. 3B and 4B, a p-type polysilicon layer 212, a conductive layer 214, an anti-fuse 216 and another p-type polysilicon layer 218 are sequentially formed over the n-type polysilicon layer 208. The p-type polysilicon layer 212 and 218 are formed, for example, by conducting an in-situ doping using boron hydride as a gaseous source. The conductive layer 214 is a tungsten silicide layer or a titanium silicide layer, for example. The conductive layer 214 is formed, for example, by conducting a low-pressure chemical vapor deposition. The anti-fuse 216 is fabricated using a material having an etching selectivity ratio higher than the p-type polysilicon layers 212, 218 and the conductive layer 214 including, for example, silicon oxide. The anti-fuse 216 is formed, for example, by conducting a low-pressure chemical vapor deposition.

[0026] The p-type polysilicon layer 212, the conductive layer 214, the anti-fuse 216 and the p-type polysilicon layer 218 are patterned to form an array of linear second stack circuits 210 each having an n-type polysilicon/p-type polysilicon/conductive layer/anti-fuse/p-type polysilicon (N/P/C/A/P) composite layer setup. The second stack circuits 220 are oriented in a direction perpendicular to and vertically above the first

stack circuits 210. In patterning the second stack circuits 220, the anti-fuse serves as an etching stop layer. Thereafter, a dielectric layer 12 is formed in the space between the second stack circuits 220. The dielectric layer 12 is, for example, a silicon oxide layer, a silicon nitride layer or a spin-coated glass layer. The dielectric layer 12 is formed, for example, by performing a high-density plasma chemical vapor deposition or a spin-coating process.

[0027] A portion of the dielectric layer 12 is removed to expose the topmost p-type polysilicon layer 218. The dielectric layer 12 above the p-type polysilicon layer 218 is removed, for example, by chemical-mechanical polishing or conducting an etching back process.

[0028] As shown in Figs. 3C and 4C, the dielectric layer 12 and the anti-fuse 206 are patterned to form an opening 14 above the conductive layer 204.

[0029] As shown in Figs. 3D and 4D, n+ polysilicon material is deposited into the opening 14 to form a plug 16. Thereafter, an n-type polysilicon layer 222, a conductive layer 224, an anti-fuse 226 and another n-type polysilicon layer 228 are sequentially formed over the p-type polysilicon layer 218. The n+ polysilicon plug 16 connects the conductive layer 204 and the n-type polysilicon layer 222 electrically. The n-type polysilicon layers 222 and 228 are formed, for example, by conducting an in-situ doping using phosphene as a gaseous source. The conductive layer 224 is a tungsten silicide layer or a titanium silicide layer, for example. The conductive layer 224 is formed, for example, by conducting a low-

pressure chemical vapor deposition. The anti-fuse 226 is fabricated using a material having an etching selectivity ratio higher than the n-type polysilicon layers 222, 228 and the conductive layer 224 including, for example, silicon oxide. The anti-fuse 226 is formed, for example, by conducting a low-pressure chemical vapor deposition.

[0030] The n-type polysilicon layer 222, the conductive layer 224, the anti-fuse 226, the n-type polysilicon layer 228 and the p-type polysilicon layer 218 are patterned to form an array of linear third stack circuits 230 each having a p-type polysilicon/n-type polysilicon/conductive layer/anti-fuse/n-type polysilicon (P/N/C/A/N) composite layer setup. The third stack circuits 230 are oriented in the same direction as the first stack circuits 210. Thereafter, a dielectric layer 18 is formed in the space between the first stack circuits 210, for example, by performing a high-density plasma chemical vapor deposition or a spin-coating process. The dielectric layer 18 is, for example, a silicon oxide layer, a silicon nitride layer or a spin-coated glass layer.

[0031] A portion of the dielectric layer 18 is removed to expose the topmost n-type polysilicon layer 228. The dielectric layer 18 above the n-type polysilicon layer 228 is removed, for example, by chemical-mechanical polishing or conducting an etching back process.

[0032] As shown in Figs. 3E and 4E, a p-type polysilicon layer 232, a conductive layer 234, an anti-fuse 236 and another p-type polysilicon layer 238 are sequentially formed over the n-type polysilicon layer 228. The p-type polysilicon layers 232 and 238 are formed, for example, by

conducting an in-situ doping using boron hydride as a gaseous source. The conductive layer 234 is a tungsten silicide layer or a titanium silicide layer, for example. The conductive layer 234 is formed, for example, by conducting a low-pressure chemical vapor deposition. The anti-fuse 236 is fabricated using a material having an etching selectivity ratio higher than the p-type polysilicon layers 232, 238 and the conductive layer 234 including, for example, silicon oxide. The anti-fuse 236 is formed, for example, by conducting a low-pressure chemical vapor deposition.

[0033] The p-type polysilicon layer 232, the conductive layer 234, the anti-fuse 236, the p-type polysilicon layer 238 and the n-type polysilicon layer 228 are patterned to form an array of linear fourth stack circuits 240 each having a n-type polysilicon/p-type polysilicon/conductive layer/anti-fuse/p-type polysilicon (N/P/C/A/P) composite layer setup. The fourth stack circuits 240 are oriented in a direction identical to the second stack circuits 220. Thereafter, a dielectric layer 20 is formed in the space between the fourth stack circuits 240 above the anti-fuse 226. The dielectric layer 20 is, for example, a silicon oxide layer, a silicon nitride layer or a spin-coated glass layer. The dielectric layer 20 is formed, for example, by performing a high-density plasma chemical vapor deposition or a spin-coating process.

[0034]
A portion of the dielectric layer 20 is removed to expose the topmost p-type polysilicon layer 238. The dielectric layer 20 above the p-type polysilicon layer 238 is removed, for example, by chemical-mechanical

polishing or conducting an etching back process.

[0035] As shown in Figs. 3F and 4F, the dielectric layer 20 and the anti-fuse 226 are patterned to form an opening 22 above the conductive layer 224. In addition, the dielectric layer 20, the dielectric layer 18 and the anti-fuse 216 are patterned to form another opening 24 above the conductive layer 214.

[0036] As shown in Figs. 3G and 4G, n+ polysilicon material is deposited into the openings 22 and 24 to form plugs 26 and 28. Thereafter, an n-type polysilicon layer 242, a conductive layer 244, an anti-fuse 246 and another n-type polysilicon layer 248 are sequentially formed over the p-type polysilicon layer 238. The n+ polysilicon plug 26 connects the conductive layer 224 and the n-type polysilicon layer 242 electrically. The n+ polysilicon plug 28 connects the conductive layer 214 and the n-type polysilicon layer 242 electrically.

[0037] The aforementioned steps may be repeated to stack alternately crossed circuits above the substrate so that a truly three-dimensional memory structure is formed.

[0038]

In this invention, a three-dimensional multi-layered memory array structure is produced. The odd-numbered memory cell array and the even-numbered memory cell array of the three-dimensional structure are alternately stacked over each other and oriented in a direction perpendicular to each other above the substrate. Hence, substrate area required to accommodate the memory device is reduced and overall

level of integration of the memory chip is increased. Moreover, in the fabrication process, the anti-fuse is used as an etching stop layer. Since the anti-fuse is fabricated from silicon oxide, the anti-fuse has a relatively high etching selectivity ratio relative to the polysilicon and the conductive layer. Therefore, the processing window is increased and the steps for fabricating the three-dimensional memory are simplified. Furthermore, the steps of forming via is to break through the anti-fuse after etching stop on the anti-fuse, so it can effectively etch stop on the conductive layer. Therefore, it can prevent via from forming p-n or n-p rectification junction due to the conductive layer being perforated, resulting in non-conducting.

[0039] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.